Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

16. (Currently Amended) A method for synchronizing a regularly occurring pulse train in frequency to the average of a bunched pulse train, the method comprising:

generating from an oscillator a plurality of differently phase shifted regularly occurring pulse trains at a given frequency;

selecting one of the regularly occurring pulse trains;

filling a FIFO memory with the bunched pulse train;

emptying the FIFO memory at [[the]] a frequency of the selected regularly occurring pulse train;

generating an error signal that represents [[the]] a state of the FIFO memory;

filtering the error signal to produce a filtered error signal;

accumulating the filtered error signal to produce a phase selection signal; and

changing the selected regularly occurring pulse train responsive to the phase selection signal so the selected regularly occurring pulse train is at [[the]] an average frequency of the bunched pulse train.

17. (Currently Amended) The method of claim 16, in which generating the plurality of differently phase shifted regularly occurring pulse trains comprises coupling a plurality of differential amplifier stages together to form a ring oscillator, the regularly

occurring pulse trains being generated by [[the]] respective stages such that each stage produces two pulse trains shifted in phase 180^0 from each other.

18. (Previously Presented) The method of claim 17, in which the coupling couples together the differential amplifier stages that have equal controllable delays.

19. (Previously Presented) The method of claim 18, in which the coupling couples eight differential amplifier stages together such that sixteen differently phase shifted regularly occurring pulse trains are generated.

20. (Previously Presented) The method of claim 19, in which the accumulating accumulates the filtered error signal at the frequency of the regularly occurring pulse trains.

21. (Currently Amended) The method of claim 16, in which the regularly occurring pulse trains have two binary values and the changing changes from one regularly occurring pulse train to another regularly occurring pulse train when both regularly occurring pulse trains have [the] a same binary value.

22. (Previously Presented) The method of claim 16, in which generating the plurality of differently phase shifted regularly occurring pulse trains comprises synchronizing the oscillator to a stable frequency reference.

23. (Previously Presented) The method of claim 22, in which the synchronizing comprises incorporating in a phase locked loop a number of counters with programmable dividing factors that determine the frequency of the regularly occurring pulse trains and programming the counters to establish a desired frequency.

24. (Previously Presented) The method of claim 23, in which the phase locked loop has a broad bandwidth.

25. (Previously Presented) The method of claim 24, in which the filtering comprises providing a control loop that has a narrow bandwidth.

26. (Previously Presented) The method of claim 16, additionally comprising adding a frequency offset to the filtered error signal prior to accumulating the filtered error signal.

27. (Currently Amended) The method of claim 26, in which the frequency offset is selected to minimize [[the]] a correction made by selecting one of the regularly occurring pulse trains.

28. (Currently Amended) A method for synchronizing a regularly occurring clock pulse train in frequency to the average of a bunched clock pulse train corresponding to data, by use of a FIFO memory having a given number of storage locations, an empty flag storage cell for each location, and a full flag storage cell for each location, the method comprising:

generating as an output signal the regularly occurring clock pulse train;

filling the FIFO memory with the data responsive to the bunched clock pulse train and emptying the FIFO memory responsive to the output signal;

setting an empty flag in the empty flag storage cell of a storage location and resetting a full flag in the full flag storage cell of the storage location when data is read out of [[the]] a corresponding storage location;

setting a full flag in the full flag storage cell of a storage location and resetting an empty flag in the empty flag storage cell of the storage location when data is written into the corresponding storage location;

summing either the empty flags or the full flags to produce an error signal that represents the state of the FIFO memory; and

changing [[the]] a frequency of the output signal responsive to the error signal so the state of the FIFO memory remains approximately constant.

29. (Previously Presented) The method of claim 28, additionally comprising adding a frequency offset to the error signal before the error signal changes the frequency of the output signal.

30. (Currently Amended) The method of claim 29, in which the frequency offset is selected to minimize [[the]] a correction made to the output signal.